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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,624	10/23/2003	Yukio Shakuda	100006-00005	5932

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ARENT FOX KINTNER PLOTKIN & KAHN
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

EXAMINER	
TRAN, MINH LOAN	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,624	SHAKUDA, YUKIO	
	Examiner	Art Unit	
	Minh-Loan T. Tran	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-10, 24-27 and 34-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-27* is/are allowed.

6)☒ Claim(s) *7,8 and 34-37* is/are rejected.

7)☒ Claim(s) *9, 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/517,121.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 08/517,121, filed on 08/21/1995.

Information Disclosure Statement

2. The information disclosure statement filed 10/23/2003 has been considered.

Oath/Declaration

3. The oath or declaration filed on 10/23/2003 is acceptable.

Drawings

4. The drawings filed on 10/23/2003 are acceptable.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 8, 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art figure 7 in view of Okazaki et al. (5,247,533).

With regard to claims 7 and 8, Applicant's prior art figure 7 discloses a method for producing a semiconductor light emitting device comprising the steps of forming an Al_2O_3 insulating substrate 51; forming a GaN buffer layer (54, 55) on the insulating substrate 51; stacking on the buffer layer (54, 55) in sequence an n-type AlGaN lower cladding layer 56, an InGaN active layer 57, a p-type AlGaN upper cladding layer 58, and a p-type GaN cap layer 59; exposing a predetermined surface of the buffer layer 55 by etching perpendicularly to the insulating substrate 51; forming electrode 60 on the p-type GaN cap layer 59 and forming electrode 61 on the exposed surface of the buffer layer 55 and separating the semiconductor wafer into plurality of LEDs by dicing. Applicant's prior art figure 7 does not disclose the steps of forming an insulating layer on the single crystal silicon substrate. However, figure 2 of Okazaki et al. discloses a method of forming light emitting device comprising the steps of forming a substrate having an insulating SiC layer 9 on a single crystal silicon layer 8 wherein the single crystal silicon layer 8 has a (111) crystal plane; and forming the stacked of GaN compound semiconductor layers (11, 12, 13) on the substrate (8, 9).

It would have been obvious to one of ordinary skill in the art to replace the insulating substrate 51 of Applicant' s prior art figure 7 by the substrate (8, 9) of Okazaki et al. in order to prevent the lattice mismatch between the GaN compound semiconductor layers and the Al_2O_3 insulating substrate.

With regard to claims 34-37, Applicant's prior art figure 7 discloses a method for producing a semiconductor light emitting device comprising the steps of forming an Al_2O_3 insulating substrate 51; forming a GaN buffer layer (54, 55) on the insulating

substrate 51; stacking on the buffer layer (54, 55) in sequence an n-type AlGaN lower cladding layer 56, an InGaN active layer 57, a p-type AlGaN upper cladding layer 58, and a p-type GaN cap layer 59; forming electrode 60 on the p-type GaN cap layer 59 and separating the semiconductor wafer into plurality of LEDs by cleaving. Applicant's prior art figure 7 does not disclose the substrate is formed of III-V group compound semiconductor material. However, figure 4 of Okazaki et al. discloses a method of forming light emitting device comprising the steps of forming a substrate 23 using III-V group compound semiconductor (i.e. GaN); forming a stacked of GaN compound semiconductor layers (24-27) on the GaN substrate 23 and forming the n-type electrode 28B on the GaN substrate 23. It would have been obvious to one of ordinary skill in the art to replace the insulating substrate 51 of Applicant' s prior art figure 7 by the n-type GaN substrate 23 of Okazaki et al. in order to obtain a good ohmic contact for n-type electrode 28B.

Allowable Subject Matter

6. Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 24-27 are allowed.

Applicant's claims 24-27 are allowable over the prior art of record because none of these references disclosed or can be combined to yield the claimed invention such as stacking GaN-compound semiconductor layers (buffer layer, lower cladding layer,

active layer, upper cladding layer and cap layer) on the II-VI compound semiconductor substrate as recited in claim 24.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh-Loan T. Tran whose telephone number is (571) 272-1922. The examiner can normally be reached on Monday-Friday 9:00 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mlt
3/2005

Minh-Loan T. Tran
Primary Examiner
Art Unit 2826